REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claim 21 is currently being amended. No new matter is added.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 19-38 are now pending in this application.

On pages 2-3 of the Office Action, claims 21-24 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,766,998 (Tseng). The Examiner states:

> Referring to figures 1-8, Tseng teaches an integrated circuit including at least one transistor, the integrated circuit comprising:
>
> A pair of local interconnects (14/16) spaced from each other (see figure 4, col. 4, lines 41-67);
>
> A gate (28) of the transistor disposed in the space between the local interconnects (14/16) and separated from each of the local interconnects by an insulating liner (24), wherein the space is less than or equal to one minimum lithographic feature (see figure 8, col. 5, lines 14-18, col. 6, lines 22-37).
>
> Regarding to claim 22, the pair of local interconnects (14/16) are spaced form each other by minimum lithographic feature (28, see figure 8).
>
> Regarding to claim 23, the insulating liners (24) are each disposed on an interconnect wall (14/16) adjacent the gate (28) to separate each of the local interconnects (14/16) from the gate (18, see figure 8).

> Regarding to claim 24, a source (30 and drain (30) are disposed by at least partially beneath the insulating liners (24, see figure 8).

Applicants respectfully traverse the rejection.

On page 3-4 of the Office Action, claims 21-23 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,943,564 (Chen). The Examiner states:

> Referring to figures 4a-4j, Chen et al. teaches an integrated circuit including at least one transistor, the integrated circuit comprising:
>
> A pair of local interconnects (poly1, 130) spaced from each other (see figure 4b, col. 3, lines 15-67);
>
> A gate of the transistor (150) disposed in the space between the local interconnects (130) and separated from each of the local interconnects by an insulating liner (142), wherein the space is less than or equal to one minimum lithographic feature (see figures 4b-4h, col. 4, lines 51-67, col. 5, lines 10-32).
>
> Regarding to claim 22, the pair of local interconnects (130) are spaced form each other by minimum lithographic feature (col. 4, lines 51-67, figure 4b).
>
> Regarding to claim 23, the insulating liners (24) are each disposed on an interconnect wall (142) adjacent the gate (150) to separate each of the local interconnects (130) from the gate (see figure 4H).

Applicants respectfully traverse the rejection. Applicants respectfully reserve the right to swear behind Tseng and Chen if necessary.

Applicants have amended claim 21 to advance prosecution. Claim 21 now recites that the width from a first end of one of the local interconnects, the first end being opposite the gate to a second end of the other of the local interconnects, the second end being opposite the gate, is less than or equal to three minimum orthographic features. This limitation is not shown, described or suggested in Chen and Tseng. The width between interconnects in Chen and Tseng is substantially greater than three lithographic features. Accordingly, it is respectfully submitted that claim 21 and its dependent claims 22-24 are patentable over Chen and Tseng.

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* * * * *

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

Date 8-17-05

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